Features

CPU

- ✓ High-performance 8051-compatible 8-bit CPU
  - 1 instruction = 1~3 machine cycle(s)
  - 1 machine cycle = 4 clock cycles (typical)
- ✓ CPU operating clock can be configured:
  - Internal clock :7.5 MHz/15 MHz/30 MHz(nominal)
  - External clock: Contact smart card input CLK supply via C3 (ISO/IEC 7816)

Memories

- ➢ FLASH
  - ✓ Size:132KB
  - ✓ Page size:512 bytes
  - ✓ Erase and program operation: Page Erase, Byte Program and Consecutive Bytes Program
  - ✓ Typical time: Erasing 2.5ms/page, Byte programming 37μs/byte, Consecutive bytes programming 5.6ms/page
  - ✓ Bit logic: 1b after erasing, 0b after programming to be 0b
  - ✓ Usage: code and data
    - Program can surmount the 64 KB limit, using CODE Banking
    - High 56 KB FLASH is accessible from XDATA
- ➢ RAM
  - ✓ Size: 2.25KB
    - 2048 bytes in XDATA
    - 256 bytes in IDATA
- ➢ OTP
  - ✓ User OTP:224bytes
  - ✓ SN:17 bytes

THC20F17BD-V40

Contact Smart Card IC

132 KB FLASH

2.25KB RAM

Preliminary

✓

Algorithms and Peripherals

- Symmetric algorithms
  - ✓ DES/T-DES
- Peripherals
  - ✓ CRC: 16-bit CRC-CCITT
  - ✓ TRNG: True Random Number Generator, for secure transactions
  - ✓ Timer: One 16-bit timer, one ETU timer

Interfaces

- ISO/IEC 7816-3 serial interface
  - ✓ UART supporting ISO/IEC 7816-3 T=0/T=1 protocol and 11 baud rates:

    F/D = 11H, 12H, 13H, 18H, 91H, 92H, 93H, 94H, 95H, 96H, 97H
  - ✓ Support GSM power consumption standards, including Clock Stop mode

Security

- ✓ Scrambling data storage
- ✓ High/low voltage and high/low clock frequency detectors
- ✓ CLK filter(ISO/IEC 7816 external clock)
- ✓ Power glitch detectors
- ✓ Security Certification: EAL4+

Work parameters

Symbol	Name	Conditions	Min	Typical	Max	Unit
T_{DES}	Time for Executing 64-bit DES Encryption	Single DES	-	17	-	clock cycle
T_{PE}	Time for Erasing a Page	-	2	2.5	3	ms
T_{BP}	Time for Program a Byte	-	33	37	41	μs

T_{DR}	Data Retention	-	10	-	-	year
N_{PE}	Page Endurance	-	100000	-	-	cycle
f_{EXT}	External Clock Freq.	-	1	-	5	MHz
f_{INT}	Internal Clock. Freq.	-	7.5	-	30	MHz
V_{CC}	Supply Voltage	-	1.62	-	5.5	V
I_{CC}	Supply Current	V_{CC}= 5.0V	-		10	mA
		V_{CC}= 3.0V	-		6	mA
		V_{CC}= 1.8V	-		4	mA
I_{SB}	Standby Current (Clock Stop)	V_{CC}= 5.0V	-		200	μA
		V_{CC}= 3.0V	-		100	μA
		V_{CC}= 1.8V	-		100	μA
T_{AMB}	Ambient Temperature	-	-25	-	85	℃
V_{ESD}	ESD Protection	HBM	4	-	-	kV

Note: This document is a Preliminary version, data and descriptions (including this table) cannot be a formal evidence for performance and functions of the IC.

Descriptions

THC20F17BD-V40 is an 8-bit CPU contact smart card IC with a total of 132 KB FLASH and hardware DES/TRNG/CRC, suitable for general IC card applications, such as SIM card, banking card, Pay-TV card, campus card, city card, etc.

COS developers can flexibly partition the 132 KB FLASH to store code and data.

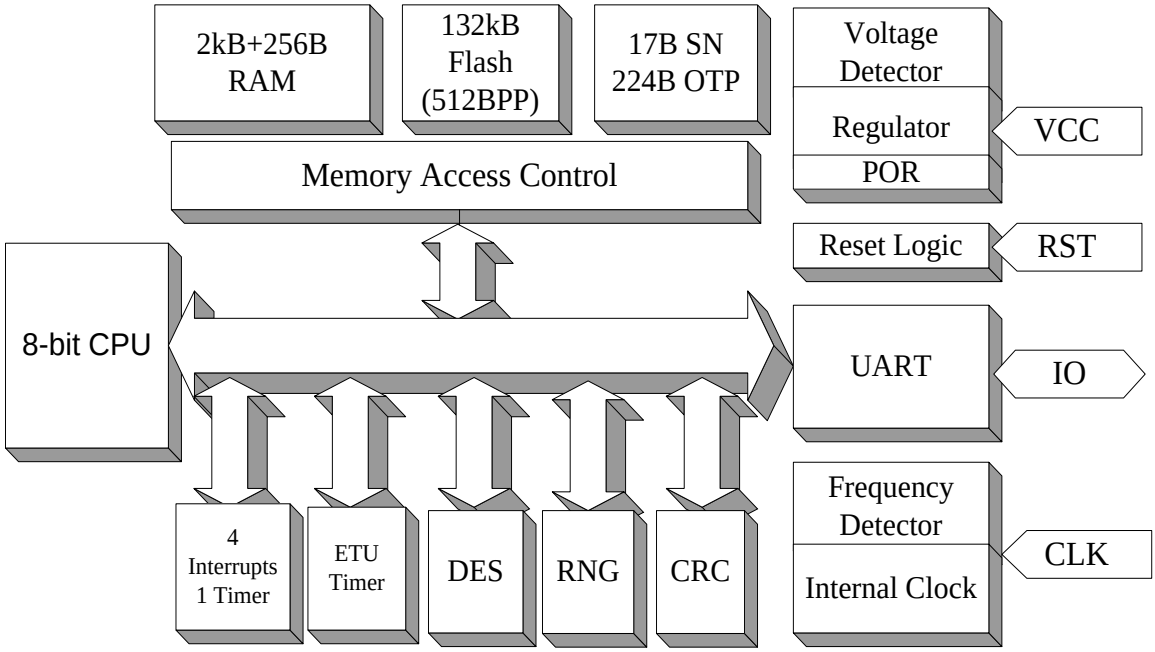
- ✓ COS can access the high 56 KB FLASH area from XDATA.
- ✓ COS can access all FLASH area from CODE, because the 64 KB limit can be surmounted by CODE banking.

To facilitate software development, the IC embeds hardware DES/ TRNG/ CRC. COS developers can enjoy smaller code size and less execution time.

For better security and reliability, the IC offers many hardware security features, e.g., high/low voltage and high/low frequency detection, etc.

THC20F17BD-V40 is fully binary compatible with THC20F17BD-V30.

Structure



Development Toolkits

- ✓ SCDS series Hardware Emulator(Target board inside)
- ✓ IDE: Keil uVision2/3/4
- ✓ Demo project and API(Application Program Interface)codes
- ✓ User Manual and Application Notes
- ✓ The UDVG software tool to generate COS downloading script with user desired format

Package and Pin Definitions

Different packages are available, e.g., wafer / module / card, etc.

Listed are pin definitions for a card package.

Signal Name	Function Descriptions	Contact defined in ISO/IEC 7816-2
VCC	Power Supply Voltage	C1
GND	Ground	C5
CLK	Clock Input	C3
RST	Reset Signal	C2
I/O	Data Input/Output	C7
NC	Not Connected	C4, C6, C8

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